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EXAMINER	
MURRAY, DANIEL C	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/672,186	GREENE, MICHAEL THOMAS	
	Examiner	Art Unit	
	DANIEL C. MURRAY	2443	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 JUN 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims 1-6** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Andreev et al. (US Patent Publication # US 2001/0018759 A1)** in view of **Rostoker et al. (US Patent # 5,742,510)** in further view of **Miura et al. (US Patent # 5,644,500).**

a) Consider **claim 1,** Andreev et al. clearly show and disclose, a computer implemented method of determining the routing (figure 2, abstract, paragraph [0002], paragraph [0088], paragraph [0091], paragraph [0096]) of interconnected regions of a routing problem (figure 11a, figure 11b, figure 11c, figure 11d, abstract, paragraph [0148]), the interconnected regions being regions of an electrical circuit (figure 1, paragraph [0015], paragraph [0033], paragraph [0034]), the method comprising: routing all connections independently and in parallel (figure 2, figure 3, abstract,

paragraph [0033], paragraph [0034], paragraph [0088], paragraph [0091], paragraph [0096]); assembling at least some contextual information about a region and the routing paths which cross in said region in the form of at least one conflict object (figure 2, figure 3, figure 8h, figure 9, abstract, paragraph [0089], paragraph [0102], paragraph [0124], paragraph [0143], paragraph [0187], paragraph [0210], paragraph [214]); and only resolving crossing conflicts only (figure 2, abstract, paragraph [0088], paragraph [0092], paragraph [0145], paragraph [0146], paragraph [0187], paragraph [0188], paragraph [0190], paragraph [0211], paragraph [0215], paragraph [0277]) when said at least some contextual information has been assembled (figure 2, figure 3, figure 8h, figure 9, abstract, paragraph [0089], paragraph [0102], paragraph [0124], paragraph [0143], paragraph [0187], paragraph [0210], paragraph [214]). However, Andreev et al. does not specifically disclose routing all connections independently and in parallel (in the sense of being fully simultaneous), each connection is routed while ignoring all other connections, or the electrical circuit is a printed circuit board electrical circuit.

Rostoker et al. show and disclose microelectronic circuit fabrication, and more specifically to an integrated circuit physical design automation system utilizing optimization process decomposition and parallel processing, wherein Rostoker et al. disclose considering all required connections independently and in parallel (figure 6, abstract, column 13 lines 52-36, column 21 lines 27-38), wherein each connection is routed while ignoring all other connections (abstract, column 14 lines 13-27, column 21 lines 27-38).

One of ordinary skill in the art at the time the invention was made would have been motivated to combine the teachings of Rostoker et al. and Andreev et al. since both concern the art of microelectronic integrated circuit design and the automation of processes thereof and as such, both are with in the same environment.

Therefore, it would have been obvious to one of ordinary skill in the art that the time the invention was made to incorporate considering all required connections in parallel independently, as taught by, Rostoker et al. into the system of Andreev et al. for the purpose of optimized placement (cell/route)(Rostoker; abstract), thereby allowing the placement or cells/ routes to have the highest fitness. However, Andreev et al. as modified by Rostoker et al. does not specifically disclose the electrical circuit is a printed circuit board electrical circuit.

Miura et al. shows and discloses a method and apparatus composing a routing processing procedure (algorithm) on the basis of predetermined routing design data (routing problem) to generate a routing program, a method and apparatus composing a placement processing procedure (algorithm) for placing components upon the routing process to generate a placement program, and a method and apparatus for determining a routing path in order to route automatically a routing pattern on a circuit board having a number of component pins, wherein Miura et al. discloses that the electrical circuit is a printed circuit board electrical circuit (abstract, column 1 lines 14-34).

One of ordinary skill in the art at the time the invention was made would have been motivated to combine the teachings of Miura et al. and Andreev et al. as modified by Rostoker et al. since both concern the art of microelectronic integrated circuit design and the automation of processes thereof and as such, both are with in the same environment.

Therefore, it would have been obvious to one of ordinary skill in the art that the time the invention was made to incorporate an electrical circuit that is a printed circuit board electrical circuit, as taught by, Miura et al. into the system of Andreev et al. as modified by Rostoker et al. for the purpose of fabricating printed circuit boards (Miura; column 1 lines 24-34), thereby allowing the user to automate the fabrication of printed circuit boards.

b) Consider **claim 3,** and **as applied to claim 1 above,** Andreev et al. as modified by Rostoker et al. as modified by Miura et al. clearly show and disclose, the method according to claim 1, comprising the steps of:

(a) defining, for each set of regions to be connected (figure 11a, figure 11b, figure 11c, figure 11d, abstract, paragraph [0148]), routing which represents a suitable manner of connecting them (figure2, abstract, paragraph [0002], paragraph [0088], paragraph [0091], paragraph [0096], paragraph [0190]), respecting only those crossing conflicts (paragraph [0145], paragraph [0146], paragraph [0187], paragraph [0188], paragraph [0211], paragraph [0215], paragraph [0277]) which have been explicitly registered with the set currently being considered (figure2, abstract, paragraph [0088], paragraph [0089]paragraph [0190]);

(b) examining connections across shared boundaries (paragraph [0148]);

(c) collating all such proposed routing and resolving any crossing conflicts (paragraph [0145], paragraph [0146], paragraph [0187], paragraph [0188], paragraph [0211], paragraph [0215], paragraph [0277]) in a symmetric manner (figure 2, abstract, paragraph [0033], paragraph [0089], paragraph [0091], paragraph [0096]);

(d) registering such crossing conflicts (paragraph [0145], paragraph [0146], paragraph [0187], paragraph [0188], paragraph [0211], paragraph [0215], paragraph [0277]) with the sets of regions which will be required to respect them on the next pass (figure 2, abstract, paragraph [0033], paragraph [0088]);

(e) repeating steps (a) to (c) until a sufficient completion and quality of routing solution is attained (paragraph [0092]); and

(f) converting the routing into suitable geometric representations of routing paths in a way which takes all desired routing into account symmetrically and simultaneously (figure 2, figure 3, figure 9, figure 10, figure 11a, abstract, paragraph [0033], paragraph [0038], paragraph [0088], paragraph [0093], paragraph [0095], paragraph [0096]).

c) Consider **claim 4**, and **as applied to claim 3 above,** Andreev et al. as modified by Rostoker et al. as modified by Miura et al. clearly show and disclose, the method according to claim 3, in which the regions are polygons (figure 11a, figure 11b, figure 11c) and the shared boundaries are edges (figure 11a, figure 11b, figure 11c, figure 11d, paragraph [0148]).

Response to Arguments

4. Applicant's arguments filed 01JUN2010 have been fully considered but they are not persuasive.

Applicant argues Andreev and Rostoker do not to teach "routing all connections of the printed circuit board electrical circuit independently and in parallel, wherein each connection is routed while ignoring all other connections"

Applicant's arguments with respect to claim 1 has been considered but are moot in view of the new ground(s) of rejection.

Applicant argues that Rostoker does not teach "routing all required connections independently and in parallel".

The Examiner respectfully disagrees; in response to Applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). While Rostoker

may teach decomposing a problem into separate processes, Rostoker still clearly discloses that those processes are performed in parallel and independently (abstract, column 21 lines 27-38) which has been thoroughly discussed in detail in previous Office Actions.

Applicant argues "that neither Andreev nor Rostoker disclose a method in which all required connections are routed in parallel and independently. Therefore, however Rostoker and Andreev are combined, there is no possibility of resulting in the present invention." and "the proposed modification cannot render the prior art unsatisfactory for its intended purpose. (MPEP §2143.01). …the proposed combination is improper".

The Examiner respectfully disagrees; the reasons and reasoning behind the combination of Andreev and Rostoker have been thoroughly discussed in detail in previous Office Actions.

Furthermore, as explained in previous Office Actions and Interviews Rostoker clearly discloses that the processes are performed in parallel and independently (abstract, column 21 lines 27-38) and therefore when incorporated with Andreev eliminate the need to require a connection to be locked down.

From Advisory Action dated 15APR2010 (and appearing in one form or another throughout the previous Office Actions)(repeated here for the convenience of Applicant):

SEE MPEP 2143 Examples of Basic Requirements of a Prima Facie Case of Obviousness which states:

The Supreme Court in KSR International Co. v. Teleflex Inc., 550 U.S. ___, ___, 82 USPQ2d 1385, 1395-97 (2007) identified a number of rationales to support a conclusion of obviousness which are consistent with the proper "functional approach" to the determination of obviousness as laid down in Graham. The key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious. The Supreme

Court in KSR noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made explicit.

Rationale that may support obviousness include applying a known technique to a known device (method, or product) ready for improvement to yield predictable results

(1) a finding that the prior art contained a "base" device (method, or product) upon which the claimed invention can be seen as an "improvement;"

Andreev is clearly a base device upon which Applicant's claimed invention can be seen as an improvement. Andreev clearly discloses substantially operating in parallel, independently, and simultaneously except in cases where there is an overlap between regions a problem which Applicant's claimed invention seeks to solve. Andreev clearly discloses routing all connections independently and in parallel (figure 2, figure 3, abstract, paragraph [0033], [0034], [0088], [0091], [0096]). Andreev clearly discloses that individual routes are considered independently (individually without regard to other routes) and in parallel (concurrently). When an overlap between regions occurs Andreev considers the routes with respect to one region and then the other, while still considered independently and in parallel they are not however considered simultaneously.

(2) a finding that the prior art contained a known technique that is applicable to the base device (method, or product);

Rostoker clearly discloses a known technique (independent, simultaneous and in parallel processing) which is the improvement which Applicant is attempting to claim. Rostoker clearly discloses a placement optimization methodology is decomposed into a plurality of cell placement optimization processes that are performed simultaneously by parallel processors on input data

representing the chip. The results of the optimization processes are recomposed to produce an optimized cell placement. The fitness of the optimized cell placement is analyzed, and the parallel processors are controlled to selectively repeat performing the optimization processes for further optimizing the optimized cell placement if the fitness does not satisfy a predetermined criterion. The system can be applied to initial placement, routing, placement improvement and other problems. Rostoker clearly discloses decomposing a cell placement/routing problem and considering everything (cell placement, routes, etc.) independently, simultaneously, and in parallel, recomposing the individual optimizations to create an optimized cell placement/routing, and then consider its overall fitness and re-evaluating as necessary until the desired fitness is achieved. Rostoker clearly discloses that connection is routed while ignoring all other connections (abstract, column 14 lines 13-27, column 21 lines 27-38). Rostoker clearly discloses decomposing cell placement/routing into a plurality of cell placement/routing optimization processes that are performed simultaneously by parallel processors and that results of the optimization processes are recomposed to produce an optimized cell placement/routing. Rostoker clearly discloses that the individual processes are considered in independently, simultaneously, and in parallel (i.e. ignoring all other connections) and then are recomposed into am optimized cell placement/routing then reevaluated as necessary.

(3) a finding that one of ordinary skill in the art would have recognized that applying the known technique would have yielded predictable results and resulted in an improved system.

The combination of Andreev and Rostoker clearly disclose routing all connections independently and in parallel, wherein each connection is routed while ignoring all other connections.

One of ordinary skill in the art at the time the invention was made would have been motivated to combine the teachings of Rostoker and Andreev since both concern the art of microelectronic integrated circuit design and the automation of processes thereof and as such, both are with in the same environment. Furthermore, Rostoker clearly discloses that the system can be applied to optimization problems in a number of diverse areas and specifically discloses that the system can be applied to routing (Rostoker; abstract, column 13 lines 47-64). Therefore, it would have been obvious to one of ordinary skill in the art that the time the invention was made to incorporate routing all required connections in parallel independently, as taught by, Rostoker into the system of Andreev because not only are they in the same field of endeavor but Rostoker also clearly discloses that the system disclosed by Rostoker can be applied not only to cell placement but also routing. In this case, one of ordinary skill in the art at the time the invention was made would have been motivated to combine the teachings of Rostoker and Andreev since both concern integrated circuit design and as such, both are with in the same environment (Andreev; paragraph [0002], Rostoker; column 1 lines 14-18), more particularly both clearly teach the routing of paths in integrated circuits (Andreev; abstract, paragraph [0015] Rostoker; column 14 lines 13-27, column 16 lines 27-40).

Furthermore, the Examiner fails to see how it would not be obvious to combine Rostoker and Andreev when by Applicant's own admission "the Rostoker parallelisation would indeed be a sensible way to implement a parallelisation framework to support the separate routing tasks described in Andreev…" while Applicant continues to argue that "...this would still not make Andreev able to route the nets fully in parallel, independently and simultaneously." the Examiner respectfully disagrees; Andreev clearly discloses the routing of interconnected regions independently, in parallel, and substantially simultaneously and Rostoker clearly discloses routing in parallel and

simultaneously and since both Andreev and Rostoker concern integrated circuit design and as such, both are with in the same environment, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate independent, parallel, and simultaneous routing, as taught by, Rostoker into the system of Andreev for the purpose of allowing all connections to be considered simultaneously.

The rationale to support a conclusion that the claim would have been obvious is that a particular known technique was recognized as part of the ordinary capabilities of one skilled in the art. One of ordinary skill in the art would have been capable of applying this known technique to a known device (method, or product) that was ready for improvement and the results would have been predictable to one of ordinary skill in the art. One of ordinary skill in the art would have been capable of applying this known techniques, as taught by Rostoker, to a known device (method, or product), as taught by Andreev, that was ready for improvement and the results would have been predictable to one of ordinary skill in the art.

Applicant argues "It is well known to skilled workers in the art that channel routing, as forms the basis of Rostoker, is simply unsuitable for PCB routing. Andreev meanwhile wholly concerns IC routing, which again is a different field to PCB routing. For the avoidance of doubt, as is well known to skilled workers in the art, PCB routing requires geometric (free space) routing, which is not disclosed either by Rostoker or Andreev. Accordingly, neither Andreev or Rostoker, considered alone or in proper combination, teaches a method suitable for PCB routing as recited in claim 1.

The Examiner respectfully disagrees; it is well known in the art that channel routing is suitable for PCB routing. The Examiner would draw attention to the teaching reference Bracha et al. (US Patent # US 6,505,331 B1)(hereafter Bracha) wherein Bracha clearly discloses "Channel routing

is used extensively in the layout of integrated circuits and printed circuit boards" (Bracha; column 1 lines 10-19). Bracha clearly discloses that channel routing is suitable for PCB routing. Furthermore, Rostoker also teaches the use of a geometric description known as a layout for the design of microelectronic circuits (column 1 lines 39-56).

With all due respect, while Applicant states "[f]or the avoidance of doubt, as is well known to skilled workers in the art, PCB routing requires geometric (free space) routing" it has become clear to the Examiner that there are many methods by used skilled workers in the art of routing design any one of which can be applied to a number of routing problems including the routing of PCBs.

Rostoker clearly discloses the automated physical design of a microelectronic integrated circuit is a specific, preferred example of simultaneous optimization processing using a parallel processing architecture to which the present invention is directed (column 1 lines 39-42) and also discloses a method of process decomposition and optimization utilizing massively parallel simultaneous processors that is especially suited to integrated circuit cell placement optimization. The present method is not limited to any specific application, however, and can be advantageously applied to optimization problems in a number of diverse areas such as logic synthesis, circuit optimization (for minimum power, etc.), software optimization, logistical problems such as traffic control and routing (column 13 lines 47-56). Rostoker clearly discloses a routing design method that is applicable to a number of optimization (routing) problems.

Miura clearly discloses a method and apparatus composing a routing processing procedure (algorithm) on the basis of predetermined routing design data (routing problem) to generate a routing program, a method and apparatus composing a placement processing procedure (algorithm) for placing components upon the routing process to generate a placement program, and a method

and apparatus for determining a routing path in order to route automatically a routing pattern on a circuit board having a number of component pins. In fabrication of recent semiconductors (LSIs), multichip modules (MCMs), printed circuit boards or the like, there are demands for high-density packaging and placement, and routing accomplished within a short period of time on the less number of signal layers. With decrease of margin (a degree of freedom) due to a trend toward high-density and high-performance as above, it becomes difficult to solve various routing problems and placement problems with one fixed algorithm. For this, it is now necessary to establish high-performance automatic routing technique and automatic placement technique (column 1 lines 14-34) and also discloses the method and apparatus of this invention are applicable to routing design or component placement design of LSIs, multichip modules, printed circuit boards, etc. (abstract).

And Bracha clearly discloses the design of electronic devices, such as integrated circuit chips and, more particularly, to the routing of nets in such chips to minimize the interconnection cost and to maximize the speed of operation and also discloses that from the prior art a number of approaches for designing very large scale integrated (VLSI) circuit chips is known especially as far as the routing of nets between the internal components of a chip are concerned. Channel routing is used extensively in the layout of integrated circuits and printed circuit boards. It is flexible enough to allow its use in various design styles such as gate-arrays, standard cells, and macro cells (column 1 lines 5-19). While the Examiner has referenced the above prior art references this is by no means an exhaustive list. Therefore, it is plainly apparent that channel routing is suitable for PCB routing.

Furthermore, in response to Applicant's argument that the references fail to show certain features of Applicant's invention, it is noted that the features upon which Applicant relies (i.e., geometric (free space) routing) are not recited in the rejected claim(s). Although the claims are

interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

The Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the Applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the Applicant, in preparing the responses, to fully consider each of the cited references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage disclosed by the Examiner.

With respect to any amendments to the claimed invention, it is respectfully requested that Applicant indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

If Applicant intends to make numerous amendments the Examiner respectfully requests that Applicant submit a clean copy of the claims in addition to the marked up copy of the claims in order to expedite the examination process.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- US 6,877,146 B1
- US 2005/0114821 A1
- US 7,305,648 B2
- US 2008/0034342 A1
- US 2008/0178139 A1
- 4,918,614
- US 6,516,447 B2
- US 2003/0126578 A1
- US 2003/0009738 A1
- US 6,886,149 B1
- US 6,957,408 B1
- US 7,017,137 B2
- US 2006/0112366 A1
- US 7,020,863 B1
- US 7,032,201 B1

- US 7,069,530 B1
- US 7,107,564 B1

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL C. MURRAY whose telephone number is 571-270-1773. The examiner can normally be reached on Monday - Friday 0800-1700 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tonia Dollinger can be reached on (571)-272-4170. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. C. M./
Examiner, Art Unit 2443

/George C Neurauter, Jr./
Primary Examiner, Art Unit 2443